International Journal of Technology Research and Management
ISSN (Online): 2348-9006
Vol 6 Issue 8 August 2019

7 T SRAM based Memory Cell Architecture for Lower Power Leakage

Surya Mishra[1], Himanshu Nautiyal[2]
Electronics & Communications, Sagar Institute of Research and Technology, Bhopal, Madhaya Pradesh, India[1, 2]
suryamishrasdl@gmail.com[1], hnautiyal11@gmail.com[2]

Abstract: *Since the past decades, CMOS devices have been reduced to achieve better performance in terms of speed, power dissipation, volume and reliability. The main area of interest in current CMOS technology is data retention and leakage reduction. SRAM (Static RAM) is the memory used to store data. Traditional static access memory (SRAM) cells suffer from an internal data instability problem because the data that is accessed is stored directly during the reading process. Noise margins in memory cells are reduced further with increased contrast and reduced power supply voltage in the changing CMOS technologies. A comparison is made between different SRAM cells based on different performance metrics, such as read delay, write delay, power dissipation, noise margin, and space in this document.*

Keywords: *SRAM, 6T RAM, 7T RAM, DRAM, VLSI.*

1. INTRODUCTION

The need of portable high-speed and low-power devices such as mobile phones, laptops, laptops, etc. It is constantly increasing. All these devices require basic memory that works and responds faster and does not need to be updated. To do this, SRAM (cache memory) is used, which functions as an important part of the modern design of the microprocessor. SRAM occupies a large part of the total area of chips and energy.

Although any of the three peripherals can be used in SRAM, MOSFETs, especially CMOS technology, are used to ensure very low levels of power consumption. Because semiconductor memories extend to very large dimensions, each cell must reach very low levels of energy consumption to ensure that the chip does not dissipate too much energy.

The VLSI chip designer must meet the strict limits of power dissipation in mobile electronics applications, such as smartphones and tablets, while adhering to computer requirements. Although wireless devices are rapidly advancing in the consumer electronics market, there is a significant handicap in mobile device design, the overall power consumption of the device, which is a trend [10]. It is also said that memories are the main cause of energy dissipation in any digital system and there is no complete digital system without memories [3].

RAM is the one where you can read sites in semiconductor memory or read them in any order, regardless of the last location of the memory accessed.

Static RAM (SRAM) found its way into almost all integrated circuits as an integrated component. Accessing information from / to a CMOS cell consumes power dynamically and consistently. The dynamic power involved in switching signals is consumed in processes such as decoding word lines, loading and unloading bit lines, amplifying discovery, and so forth. Static power is consumed when there is a direct path from the VDD to the ground while accessing memory [1].

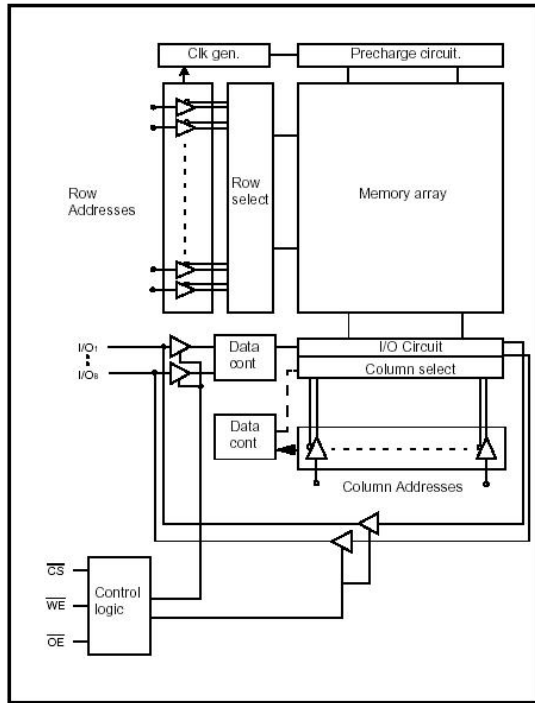


Fig 1:Functional Block Diagram of SRAM

The circuit of the individual SRAM cell contains four transistors configured as cross-reflectors. In this format, the circle contains two stable states, and these are equal to "0" and "1". In addition to the four transistors in the core memory cell, additional transistors are required to control access to the memory cell during read and write operations. This makes a total of six transistors, which is called a 6T memory cell. Sometimes additional transistors are used to provide 8T or 10T memory cells. These additional transistors are used for functions such as executing additional ports in a log file, etc., for SRAM memory.

Low voltage operation at SRAM faces many challenges, resulting from process variability of bit-cell stability, detection, engineering, and efficient CAD methodologies. The trend towards increased SRAM included in the measured technology exacerbates the specific need for SRAM in low power systems. More memory on the chip provides an effective way to use silicon because of low memory density, regularity of design, performance and power benefits to reduce bandwidth outside the chip. As a result, the incremental integration of embedded SRAM continues.

In the traditional SRAM 6AM cell, the non-destructive reading process condition and the authoritative write operation are met by resizing all the transistors in the SRAM cell correctly. The size is based on the ratio of cells (CR) [6] and the lift rate (PR) [6] of the transistor.

2. 7T SRAM

The technology and the electrical voltage scale continue to improve the logic circuit delay with each generation of technology. However, the speed of the PES is increasingly limited by the delay of the signal in long interconnects and very charged bit lines due to increase in capacitance and resistance [1]. Static RAM (SRAM) is a type of semiconductor memory that uses installable closing circuits to store every bit. SRAM shows data stability, but it is still volatile in the traditional sense of data loss when memory does not receive power. The stability and SRAM space must be a concern in the SRAM cell design. The SRAM must be able to write, read, and save data during the power application. The main challenge in designing a SRAM cell is to ensure that circuits that maintain the condition are weak enough to overcome them while typing, and strong enough not to be disturbed during the reading process. For almost 40 years, CMOS devices have been reduced to achieve higher speed, performance and lower power consumption. Due to its high speed, the SRAM-based cache and system are used in chips. New SRAMs have been introduced for higher noise margin with better performance. In most of these read and write processes, these cells are isolated to obtain a greater margin of noise. SRAM represents a large portion of the chip, and is expected to grow in the future in both high-performance mobile devices and processors. To achieve a longer battery life and greater reliability for mobile applications, the low-power SRAM range is a necessity [2]

The SRAM 7T circuit is made up of two CMOS reflectors connected to each other by an additional NMOS transistor connected to the read line and has NMOS transistors connected to the bit lines and the line bar of the bits, respectively. Figure 2 shows the SRT 7T cell circuit, where the MN3 (WL) pass-through transistors are connected to the access writing procedure and the MN4 is connected to the read line (R) to perform read operations in the column bit lines (BL and BLB). Bit lines act as an I / O port that moves data from SRAM cells to a speaker to detect during the read process, or from writing to memory cells during write operations. All transistors have a minimum length (LMIN = 45 nm depending on the technology used), while their offerings are usually design parameters. The value of WP1 and WP2 determine the width of the PMOS and WN1 transistors. WN2 is defined as the width of the NMOS

controller transistors in the CMOS adapters, while WN3 and WN4 are the width of the transistors.

- **Features**
  - 23% smaller than Conv. 6T bitcell
  - Low VDD(440mV)
  - Not suit for low speed demand
  - 90% power saving
  - Low write power
  - SNM is effected by "Read pattern"

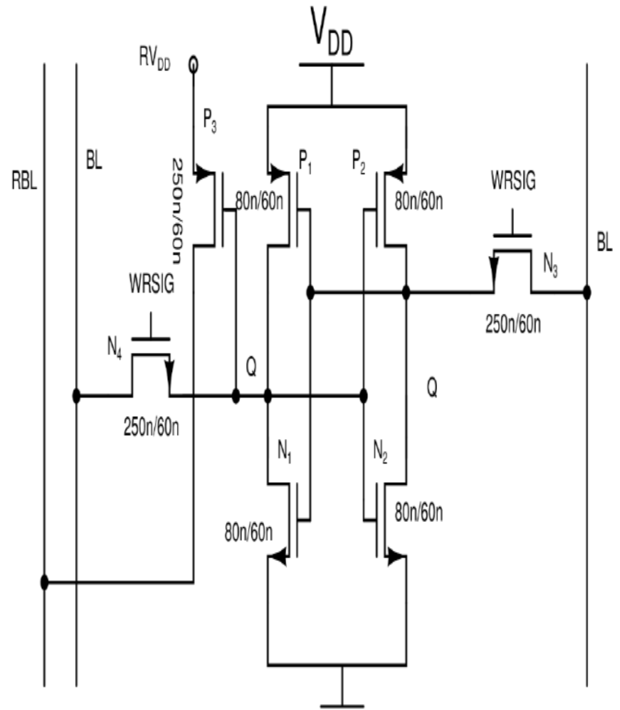
  (Read 0-N2,P2,N4& Read 1-N1,P1,N3,N5)
  - 17.5% larger than 6T
- **Approaches**
  - Separate Read &Write WL
  - Separate Read &Write BL
  - Data protection nMOS:N5
  - BL swing: VDD/6
  - Reducing write power by cut off

  the (feedback) connection to BL
  - **Performance**
  - 20ns access time@0.5V
  - 90nm process
  - 0.35um process
  - Leakage not controlled well
  - 0.18um process
  - 49% write power saving

In all the cells analyzed so far, the primary storage element that forms the building block of the SRAM cell is the inverter for cross-coupling. As improvements, additional transistors were added to the notes path of the bit cell to separate read and write operations. Unfortunately, none of the SRAM cells discussed so far have considered the variance of the uneven process when designing the SRAM cell. One of the most common ways to handle the variation of processes is to use the transistor size, but when it comes to the process of supplying a very low voltage, the use of transistor size to improve transistor tolerance tolerance affects the operation of the SRAM cell stability.

Proposed 7T SRAM cell

1. Proposed 7T SRAM cell in a 65nm CMOS technology is shown in Fig. with sizing of individual transistor.
2. An area efficient and low leakage power 7T SRAM cell is presented.
3. Separate data access mechanisms is provided for the read and write operations in the proposed 7T SRAM.



1. Similar to all conventional SRAM cells, back to back inverters are used for data storage.
2. Access transistors N3 and N4 is controlled by write signal (WRSIG). The operation of P3 is controlled by RBL, RVDD (Read signal) and by the data present in the cell.
3. Leakage power reduced further in proposed 7T with super cut-off word lines.
4. Applied negative voltage to the word lines in this architecture. This negative voltage made gate to source voltage of NMOS transistor less than zero.
5. So, proposed method with super cut-off bit lines reduces sub threshold current through access transistors.

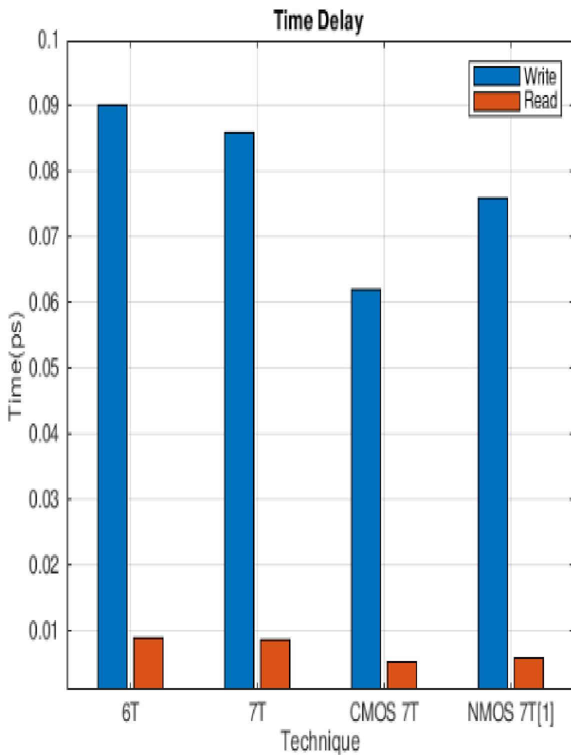
3. RESULT ANALYSIS

The simulation has been done in Verilog and VHDL. Result has been calculated in three parameters. The results seem to be that the proposed method gives batter results.

Table 1: Time Delay

	6T	7T	NMOS 7T[1]	CMOS 7T
R	0.009	0.0087	0.0068	0.0054
W	0.09	0.086	0.076	0.062

The table show the difference of time delay with both type of memory. It seems to be that the proposed method gives the less time delay. It shows the access speed of the memory.

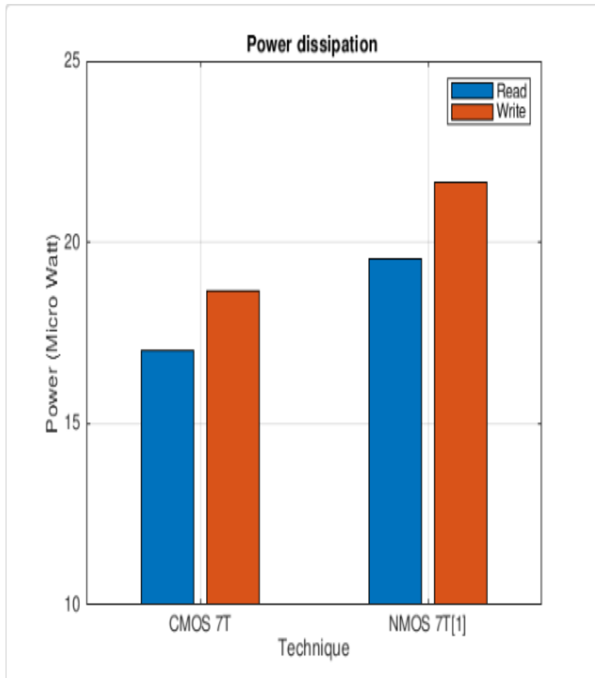


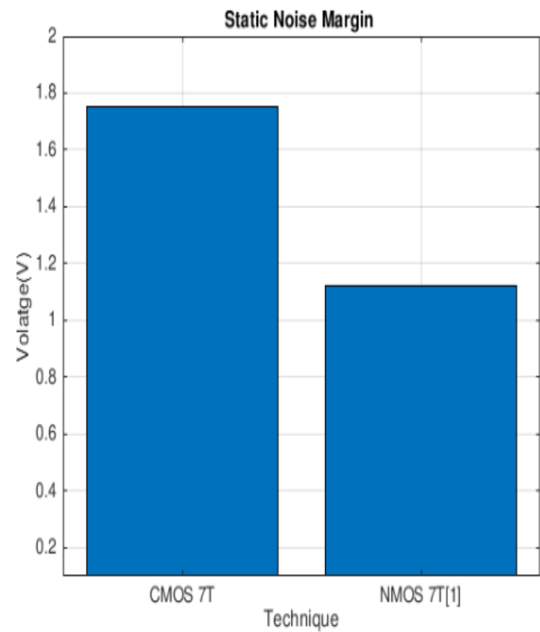
Power Dissipation

Energy dissipation means the total energy that a component transmits in all its forms. Because of the energy conservation, this has the same total energy value that is electrically connected to it.

	NMOS 7T[1]	CMOS 7T
R	19.56	17
W	21.65	18.67

Both the table and graph show the results regarding power Dissipation. It shows the proposed approach gives the batter results.





Static Noise Margin

The static noise margin (SNM) is the most important parameter for memory design. SNM, which affects both the reading margin and the write margin, is associated with the threshold voltage of the NMOS and PMOS of the SRAM cell, which is why we analyzed SNM with the read margin, the write margin, and the threshold voltage.

NMOS 7T[1]	CMOS 7T
1.12	1.75

The results in Table 1, 2 and 3 were obtained after simulating SRAM structures using a 120 nm technique. The three important parameters obtained from simulations are SNM, write delay and power dissipation. Analysis of the simulation results reveals that the proposed technique provides an improvement to the delay of writing in both cases of SRAM 7T, and therefore, it can be said that it will also show a marked improvement in other cases.

4. CONCLUSION

Proposed 7T SRAM cell plays an important role where stability, leakage power and area cannot be compromised while designing memory circuits. 7T SRAM cell architecture introduced in this work has separate read and write paths. Proposed architecture eliminates direct read access by isolating data storage nodes from the bit lines. Proposed 7T has almost same leakage power consumption as that of 6T SRAM cell. Proposed architecture will be reduced leakage power present in conventional 7T SRAM. In this dissertation CMOS based 7T SRAM cell is proposed. The presented cell had an extra CMOS transistor connected in parallel with ground transistor compared to conventional 6T. With this transistor the leakage current during hold operation can be limited and discharging the storage node gets accelerated. The proposed cell performs better in both read and write

operation. In future work move to uniform read and write operational cost.

REFERENCES

[1] K. Roy and S. Prasad, Low Power CMOS VLSI Circuit Design, 1st ed. New York: Wiley, 2000

[2] Y. J. Chang, F. Lai, and C. L. Yang, "Zero-Aware Asymmetric SRAM Cell for Reducing Cache Power in Writing Zero," IEEE Transactions on Very Large Scale Integration Systems, vol. 12, no. 8, pp. 827-836, 2004.

[3] G. Wann et al., "SRAM cell design for stability methodology", in Proc. IEEE VLSI-TSA, pp. 21-22, April 2005

[4] Jain and S. Sharma, "Optimization of Low Power 7T SRAM Cell in 45nm Technology," 2012 Second International Conference on Advanced Computing & Communication Technologies, Rohtak, Haryana, 2012, pp. 324-327.

[5] S. Akashe, S. Rastogi and S. Sharma, "Specific power illustration of proposed 7T SRAM with 6T SRAM using 45 nm technology," International Conference on Nanoscience, Engineering and Technology (ICONSET 2011), Chennai, 2011, pp. 364-369.

[6] B. Rawat, K. Gupta and N. Goel, "Low Voltage 7T SRAM cell in 32nm CMOS Technology Node," 2018 International Conference on Computing, Power and Communication Technologies (GUCON), Greater Noida, Uttar Pradesh, India, 2018, pp. 238-241.

[7] Venkatareddy, R. Sithara, Y. B. N. Kumar and M. H. Vasantha, "Characterization of a Novel Low Leakage Power and Area Efficient 7T SRAM Cell," 2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID), Kolkata, 2016, pp. 202-206.

[8] S. H. Kumar and B. S. Kariyappa, "Analysis of low power 7T SRAM cell employing improved SVL (ISVL) technique," 2017 International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT), Mysuru, 2017, pp. 478-482.

[9] K. F. Sharif, R. Islam, M. Haque, M. A. Keka and S. N. Biswas, "7T SRAM based memory cell," 2017 International Conference on Innovative Mechanisms for Industry Applications (ICIMIA), Bangalore, 2017, pp. 191-194.

[10] Y. Huang, M. Chiang, S. Wang and S. K. Gupta, "An area efficient low-voltage 6-T SRAM cell using stacked silicon nanowires," 2018 International Conference on IC Design & Technology (ICICDT), Otranto, 2018, pp. 117-120.

[11] Y. -. Lee, J. H. Lee, Y. S. Tsai, S. Mukhopadhyay and Y. F. Wang, "Modeling of BTI-aging V<inf>T</inf> stability for advanced planar and FinFET SRAM reliability," 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Kamakura, 2017, pp. 85-88.

[12] B. K. Madhavi and T. V. Reddy, "Design strategy & analysis of Subthreshold SRAM in power & delay for wearable applications," 2017 2nd International Conference on Communication and Electronics Systems (ICCES), Coimbatore, 2017, pp. 872-878.

[13] A. Venkatareddy, R. Sithara, Y. B. N. Kumar and M. H. Vasantha, "Characterization of a Novel Low Leakage Power and Area Efficient 7T SRAM Cell," 2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID), Kolkata, 2016, pp. 202-206.

[14] M. Moghaddam, M. H. Moaiyeri and M. Eshghi, "Ultra low-power 7T SRAM cell design based on CMOS," 2015 23rd Iranian Conference on Electrical Engineering, Tehran, 2015, pp. 1357-1361. doi: 10.1109/IranianCEE.2015.7146428

[15] J. Liu, M. B. Clavel and M. K. Hudait, "An Energy-Efficient Tensile-Strained Ge/InGaAs TFET 7T SRAM Cell Architecture for Ultralow-Voltage Applications," in IEEE Transactions on Electron Devices, vol. 64, no. 5, pp. 2193-2200, May 2017.